CS20 System Guide: Getting Started

Part Number: 51-0064-1B

© 2000 API NetWorks, Inc. All rights reserved.

Part #: **51-0064-1B**

Date: **6/15/2001**

API NetWorks, Inc.
130C Baker Avenue Extension
Concord, MA 01742
Tel: 978.318.1100
Fax: 978.371.3177

API NetWorks, Inc. reserves the right to make changes in its products without notice in order to improve design or performance characteristics.

This document is considered to be preliminary with further revisions and corrections in process. API NetWorks, Inc. makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication or the information contained herein, and reserve the right to make changes at any time, without notice. API NetWorks, Inc. disclaims responsibility for any consequences resulting from the use of the information included in this publication.

This publication neither states nor implies any representations or warranties of any kind, including but not limited to, any implied warranty of merchantability or fitness for a particular purpose. API NetWorks, Inc. products are not authorized for use as critical components in life support devices or systems without API NetWorks, Inc.'s written approval. API NetWorks, Inc. assumes no liability whatsoever for claims associated with the sale or use (including the use of engineering samples) of API NetWorks, Inc. products except as provided in API NetWorks, Inc.'s Terms and Conditions of Sale for such products.

Trademarks

Product names used in this publication are for identification purposes only and may be trademarks of their respective companies.

Preliminary Product Information

The information in this publication is preliminary, and is believed to be accurate at the time of publication. API NetWorks, Inc. makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication or the information contained herein, and reserves the right to make changes at any time, without notice.

Revision History

Date	Rev	Description
Oct 2000	1.0	Initial release.
Jan 2001	1.1	Engineering updates.
April 2001	1.2	CE compliance notification and installation requirements added.
June 2001	1.3	Engineering updates.

Table of Contents

Revision History **iii**

Table of Contents **iv**

List of Tables . . . vi
List of Figures . . . vii

European Community Customers **viii**

Preface **ix**

Overview . . . ix
Audience . . . ix
Scope . . . ix
Organization of the Information . . . ix
Conventions and Definitions . . . x
Typographic Conventions . . . x
Signals and Bits . . . x
Data . . . x
Acronyms . . . xi

Chapter 1 Introduction **1-1**

1.1 Features . . . 1-1
1.2 System Components . . . 1-3
1.2.1 Enclosure . . . 1-3
1.2.2 Front View of the System . . . 1-3
1.2.3 Rear Panel of the System . . . 1-4
1.2.4 Internal Power Failure . . . 1-5
1.2.5 Memory . . . 1-5
1.2.6 Alpha 21264 Processors . . . 1-6
1.2.7 PCI Riser . . . 1-6
1.2.8 I/O Board . . . 1-6

Chapter 2 Firmware Platform **2-1**

2.1 Supported Firmware . . . 2-1
2.1.1 Operating System . . . 2-1
2.1.2 SROM Code . . . 2-1
2.1.3 Alpha Diagnostics . . . 2-1
2.1.4 Alpha SRM Console . . . 2-2

Chapter 3 System Memory **3-1**

3.1 Memory Subsystem . . . 3-1

3.2 Configuring SDRAM Memory 3-1

Chapter 4 System Troubleshooting 4-1

4.1 Error Recovery 4-1
4.1.1 Error Conditions 4-2
4.1.2 Restore Factory Defaults 4-2
4.1.3 Reload Firmware 4-3
4.1.4 Error Recovery Procedure 4-3

Appendix A Resources A-1

A.1 Customer Support A-1
A.2 Supporting Products A-1
A.3 Alpha Products A-1
A.4 Documentation A-2

Index I-1

List of Tables

Table: 1-1 CS20 Product Features 1-2
1-3 Rear LED Status Indicators 1-5
1-2 Front LED Status Indicators 1-5
3-1 CS20 SDRAM Memory Configurations 3-2
4-1 J2 Pin Functions 4-2
4-2 Jumper Settings for Error-Recovery Procedures 4-3

List of Figures

Figure: 1-1 CS20 Logical Block Diagram 1-1
1-2 Front View of the CS20 System 1-4
1-3 Rear View of the CS20 System 1-4
4-1 J2 Firmware Configuration Jumper Block 4-1

European Community Customers

The CS20 is designed for professional use in cluster applications.

CS20 clusters deployed in European Community (EC) countries must be configured with a minimum of four (4) CS20s to meet the requirements of EN61000-3-2.

API NetWorks has certified and labeled the CS20 as European Conforming (CE) compliant based on the minimum four (4) node installation requirement.

CS20 installation procedures also require that the CS20 power supply is connected to a properly grounded, single-phase AC power outlet.

Please email any questions regarding this issue to:

customer.support@api-networks.com

Or, contact your API NetWorks sales representative.

Preface

Overview

This guide describes the API NetWorks, Inc. CS20 system including the dual Alpha 21264 microprocessor / Compaq 21272 core logic chipset motherboard; the CS20 PCI riser; and the high-density 1u form factor CS20 chassis.

Note: *In this document, the designation 21264 refers to the 21264B processor.*

Audience

This guide is intended for system integrators and others to evaluate and use computer systems based on the CS20 system.

Scope

This guide describes the firmware platform and memory interfaces of the CS20 system. This manual does not include specific details on industry standards (for example, on PCI bus specifications). Additional information is available in the appropriate vendor and IEEE specifications. See Appendix A for information on related documentation.

Note: *For complete information on using the SRM console, displaying system configurations, and Linux operating system installation, refer to the API NetWorks Firmware Reference Guide, 51-0058-1A.*

Organization of the Information

This guide is organized as follows:

- Chapter 1, “Introduction,” is a summary of the features and implementation of the CS20.
- Chapter 2, “Firmware Platform,” includes a description of the firmware components supported by the CS20 and the order in which these components load.
- Chapter 3, “System Memory,” discusses CS20 system memory and address mapping.
- Chapter 4, “System Troubleshooting,” discusses basic hardware and software troubleshooting for the CS20 system.
- Appendix A, “Resources,” describes how to obtain technical information and support for the CS20, and where to order parts and accessories for the CS20.

Conventions and Definitions

This section defines product-specific terminology, acronyms, and other conventions used throughout this guide.

Note: *Notes highlight information that will ease tasks related to the assembly and operation of the system.*

CAUTION: A Caution describes potential hazards that may damage equipment, data, or software. Measures that the user can take to guard against the damage are included as well.

WARNINGS: A Warning points to situations that pose the threat of personal injury or the risk of irreversible destruction of the data or the operating system.

Typographic Conventions

This guide uses the following type conventions:

- Variable information and document titles appear in *italic* type.
- Text that you type is shown in **`bold Courier font`**.
- Type that appears on a screen, such as an example of computer output, is shown in `Courier font`.
- Two key names joined with a forward slash are simultaneous keystrokes. Press down the first key while you type the second key, as in press Ctrl/S.

Signals and Bits

- Signal Ranges—In a range of signals, the highest and lowest signal numbers are contained in brackets and separated by a colon (for example, D[63:0]).
- Reserved Bits and Signals—Signals or bus bits marked *reserved* must be driven inactive or left unconnected, as indicated in the signal descriptions. These bits and signals are reserved by API NetWorks, Inc. for future implementations. When software reads registers with reserved bits, the reserved bits must be masked. When software writes to these registers, it must first read the register and change only the non-reserved bits before writing back to the register.

Data

The following list defines data terminology:

- Units
  - A *word* is two bytes (16 bits)
  - A *doubleword* is four bytes (32 bits)
  - A *quadword* is eight bytes (64 bits)

- Addressing—Memory is addressed as a series of bytes on eight-byte (64-bit) boundaries in which each byte can be separately enabled.
- Abbreviations—The following notation is used for bits and bytes:
  - Kilo—K, as in 4-Kbyte page (2^{10})
  - Mega—M, as in 4 Mbits/sec (2^{20})
  - Giga—G, as in 4 Gbytes of memory space (2^{30})

Acronyms

The following is a list of the acronyms used in this guide and their definitions.

Acronym	Meaning
BIST	Built-In Self Test
CE	European Conforming
CLI	Command Line Interface
CSR	Control/Status Register
CPU	Central Processing Unit
cUL	Canadian Underwriters Laboratory
DIMM	Dual Inline Memory Module
DRAM	Direct Random Access Memory
DQM	Data Input/Output Mask
ECC	Error Checking and Correcting/Error Checking Code
EIDE	Enhanced Integrated Device Electronics
EMI	Electromagnetic Interference
EPLD	Electrically Programmable Logic Device
ESBGA	Enhanced Super Ball Grid Array
FCC	Federal Communications Commission
FDC	Floppy Disk Controller
FDD	Floppy Disk Drive
FID	Frequency Identification
FIFO	First In, First Out
FPGA	Field Programmable Gate Array
HDD	Hard Disk Drive
I^2C	Inter-integrated Circuit
IDE	Integrated Device Electronics
I/O	Input/Output

Acronym	Meaning
ISA	Industry Standard Architecture
LED	Light Emitting Diode
LVD	Low Voltage Differential
LVTTL	Low Voltage Transistor-Transistor Logic
OS	Operating System
PAL	Privileged Architecture Library
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PIO	Programmed Input/Output
PLL	Phase Locked Loop
ROM	Read-only Memory
SCSI	Small Computer System Interface
SDRAM	Synchronous Direct Random Access Memory
SPD	Serial Presence Detect
SROM	Serial Read-only Memory
SRAM	Static Random Access Memory
SRM	System Reference Manual
SSRAM	Synchronous SRAM
TIG	TTL Integrated Glue Logic
UL	Underwriters Laboratory
USB	Universal Serial Bus
VRM	Voltage Regulator Module

Chapter 1 Introduction

This chapter provides an overview of the CS20 product, including the features and components. The CS20 is a rack-mounted Alpha Processor system designed for optimal performance in a cluster application.

CAUTION: Always take appropriate electrostatic discharge safety measures when handling boards or modules.

1.1 Features

Figure 1-1 illustrates the logical block diagram for the CS20 system.

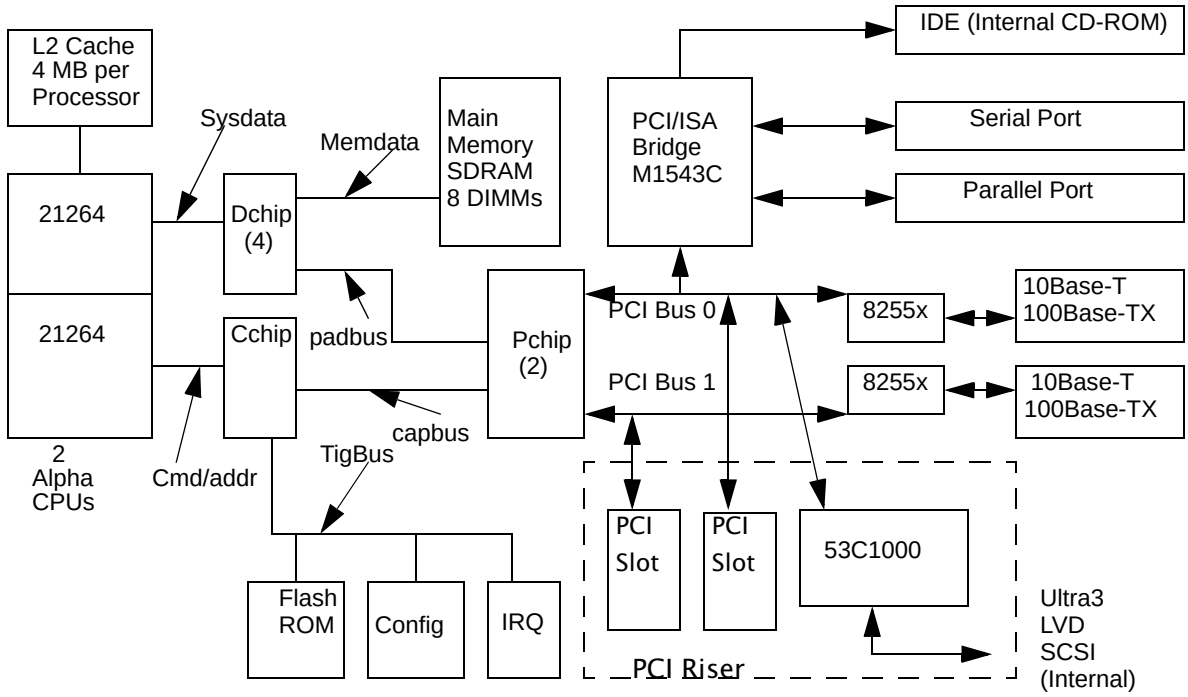

Figure 1-1 CS20 Logical Block Diagram

Table 1-1 summarizes the CS20 product features.

Table 1-1 CS20 Product Features

Feature	Description
Physical Form Factor:	• High-Density (1.75 inch x 17 inches x 20 inches) • Alpha 21264B at speeds of 833 MHz
Chipset:	21272 (Tsunami)—One Cchip, four Dchips, and two Pchips provide the following: • Maximum 166 MHz system bus with Double Data Rate (DDR) transfers, maximum bandwidth of 2.67 GBytes/second. • One 256-bit memory bus. • Two 64-bit, 33 MHz PCI buses.
Cache:	External L2 cache with 128-bit data path supports: • 4 MB cache per processor, DDR SRAMs.
Main Memory:	• Eight 168-pin Dual Inline Memory Module (DIMM) sockets, up to 2 GB (256 MB per DIMM). • Supports Phase Locked Loop (PLL) or Register-based Synchronous Direct Random Access Memory (SDRAM) Serial Presence Detect (SPD) modules of 64 MB, 128 MB, and 256 MB. • Low-Voltage Transistor/Transistor Logic (LVTTL) compatible memory I/O.
Power:	500W PSU: (+) 12 Vdc and standby (+) 5 Vdc. Supplies all integrated devices and up to 10A to PCI slots (25W) and 2A to internal disk drive (25W).
On-board I/O:	• M1543C-B1E PCI/ISA Bridge (*PCI Local Bus Specification Revision 2.2* compliant) and Enhanced Integrated Device Electronics (EIDE) controller. • Ultra160 SCSI Controller (Adaptec AIC-7892 on current revision, Symbios 53C1000 on earlier revisions) • Dual 10/100 Fast Ethernet network controllers.
I/O Slots:	Two 64-bit, 33 MHz PCI Slots, PCI Local Bus Specification Revision 2.1 compliant.
Firmware:	SROM, Alpha Diagnostics, and SRM.

Table 1-1 CS20 Product Features (Continued)

Feature	Description
System Management (via PCI-ISA Bridge I^2C Controller):	• Monitoring of processor and motherboard voltages. • Processor and system thermal monitors. • Detection of processor and motherboard presence, versions, and asset record. • Detection of system and power-supply status and power-supply inhibiting. • Indication of system error for both hardware- and software-detected problems • Monitoring of system fan speeds.

1.2 System Components

The CS20 system is implemented in industry-standard parts and uses two 21264 central processing units (CPUs).

1.2.1 Enclosure

The enclosure components for the CS20 system are described in this section.

- **Physical Dimensions.** The system enclosure measures 1.75 inches high by 17 inches wide by 20 inches deep.
- **Fans.** There is a total of 11 fans in the CS20 system: five on the front of the system connected by cables to the system motherboard, and six mounted internally.

  Two of the six internal fans cool the PCI card assembly and are cabled onto the PCI riser; one fan cools the I/O and is cabled onto the motherboard; three fans on the back of the system cool the power supply.
- **Bezel.** The system has a removable front bezel. See the *CS20 Quick Start Installation Guide, 51-0064,* for information about removing and replacing the bezel.
- **Power Supply.** The CS20 system is equipped with a 500-Watt AC Power 100-120/200-240VAC 60/50 Hz power supply.
- **Disk Carrier.** The system includes a custom mounting kit that allows the installation of a one-inch-high SCA SCSI disk drive.

1.2.2 Front View of the System

The front panel of the CS20 system contains five fans with connectors to the motherboard, a Slimline CDROM drive, a hard disk drive bay, and three LEDs.

Note: *See Table 1-2 for information on interpreting the system front LEDs and Table 1-3 for information on interpreting the system rear LEDs.*

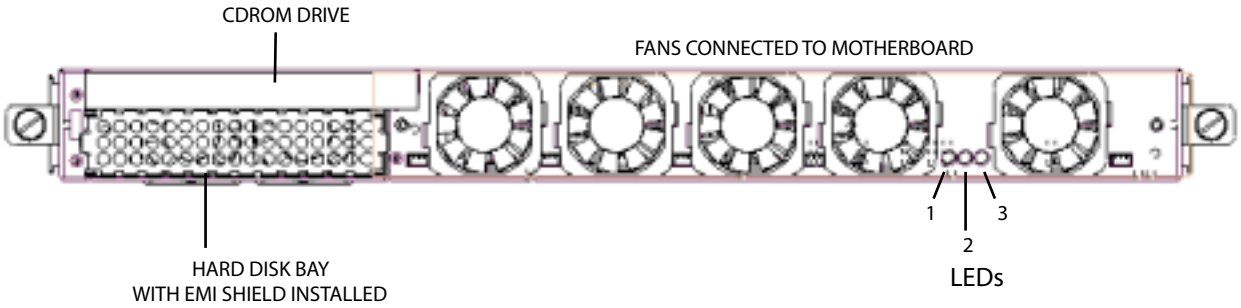

Figure 1-2 Front View of the CS20 System

1.2.3 Rear Panel of the System

The I/O rear panel contains the Dual Ethernet connectors and the parallel and dual serial connectors.

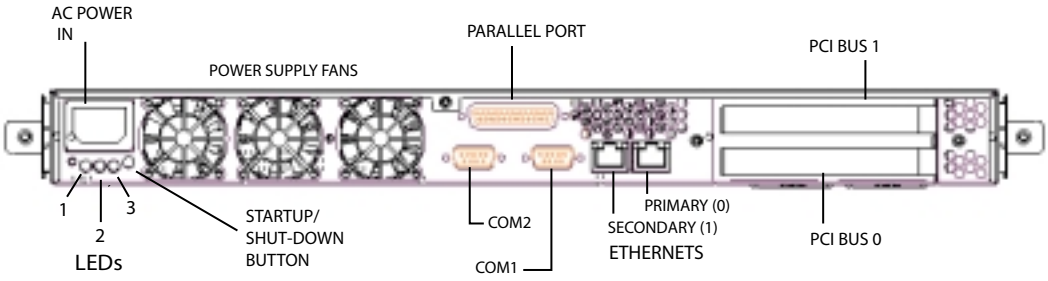

Figure 1-3 Rear View of the CS20 System

The CS20 has front and rear LED status indicators.

Table 1-2 Front LED Status Indicators

LED	Indication
1	• Steady Red when system failure needs attention. • Off when the system is functioning properly.
2	Blinks Amber to indicate system activity.
3	• Blinks Green when the system is in Standby mode. • Glows Green to indicate that system power is on.

Table 1-3 Rear LED Status Indicators

LED	Indication
1	• Steady Red when a system failure needs attention. • Off when the system is functioning properly.
2	Blinks Amber to indicate system activity.
3	• Blinks Green when the system is in Standby mode. • Glows Green to indicate that system power is on. • Glows Red when the system power has failed.

1.2.4 Internal Power Failure

In the event of an internal power failure, clear the Red Power Fail LED with these steps:

1. Unplug the AC power cord. The main AC must be removed to clear the indication. Manual, remote and automatic wake up have no effect.
2. Replug the AC power cord.
3. Leave Stand-By Power on.
4. If the Red Power Fail state persists, contact Customer Support.

1.2.5 Memory

The CS20 system motherboard has two 833MHz Alpha 21264 processors. There are 4MB DDR L2 cache per processor. L2 cache bandwidth is 8.9 GB/s @ 833 MHz.

The CS20 motherboard has eight DIMM sockets arranged in two banks: Bank 0 and Bank 1. Each bank has four sockets and provides a 256-bit wide data path. DIMMs in the same bank must be the same type, size, and speed. DIMMs in

different banks may differ in type, size, and speed. Bank 0 must be filled for the CS20 motherboard to work.

Note: *For detailed information on installation and removal, refer to the CS20 Quick Start Guide, 51-0064.*

1.2.6 Alpha 21264 Processors

The processors are soldered into place on the motherboard. The Alpha processors have a heat sink attached with an integral heat pipe for maximum heat dissipation.

1.2.7 PCI Riser

PCI expansion capabilities include dual independent peer-to-peer 64-bit PCI buses providing a total of 528 MB/s I/O bandwidth. There are two 64-bit 33-MHz PCI slots, each on a separate bus. Internal Ultra3 SCSI and PCI fans are connected to the PCI riser.

The riser also contains:

- the Ultra160 controller
- a connector for the SCSI cable
- a multi-function environmental monitor
- fan connections for the PCI area

1.2.8 I/O Board

I/O integrated expansion capabilities include two serial ports with modem control, two 10/100 Mb/s Ethernet connectors with integrated LEDs, and one parallel port connector.

Chapter 2 Firmware Platform

This chapter describes the CS20 target operating system (OS), the SROM code, Alpha Diagnostics, and Alpha SRM Console firmware. The order in which firmware loads is described as well.

Note: *For complete information on using the SRM Console, displaying system configurations, and Linux operating system install which is available at* `www.api-networks.com`.

2.1 Supported Firmware

The CS20 product supports the following firmware versions:

- SROM code (version 2.0 or higher)
- Alpha Diagnostics (version 1.4 or higher)
- Alpha SRM Console (version A5.8 or higher)

2.1.1 Operating System

The CS20 system supports Linux kernels 2.2.18 or higher.

Note: *Refer to product support at* `www.api-networks.com` *for current information on specific distributors and OS versions supported by the CS20 product.*

2.1.2 SROM Code

When the CS20 is turned on or reset, SROM code automatically loads into Icache in each CPU. The SROM code then:

1. Initializes CPU.
2. Detects configuration jumpers and CPU memory configuration.
3. Initializes chipset values, including memory timing, Cchip, Dchip, and Pchip registers.
4. Performs power-on self test (POST) of basic system needed to run Alpha Diagnostics (memory, etc.).
5. Initializes system memory.
6. Initializes L2 cache.
7. Loads the Alpha Diagnostics firmware.

2.1.3 Alpha Diagnostics

SROM code uses the 21264 Debug ports for POST error reporting. The Debug ports for

the CPUs share the serial port 9-pin DIN connector on the system rear with the system COM1/COM2 UARTs.

SRM Console and the operating system kernels require that various system components be functioning correctly. Alpha Diagnostics completes the POST of interrupts, console I/O, PCI devices, and the next-level firmware. In the absence of system errors, Alpha Diagnostics leads the next level of system firmware installed in the system ROM (SRM Console).

When basic POST detects problems (and for extended self-testing), Alpha Diagnostics includes tests of:

- Interrupt handling, which raises interrupts with a known response.
- CS20 motherboard components, including chipset, Flash ROM integrity, and on-board devices.
- Memory, which includes stress test.
- PCI bus, which includes initialization, stressing, and interrupts.
- System Management (SM) timer support and EEPROMs.
- DMA access test.
- Flash ROM management and recovery.

Alpha Diagnostics uses the COM1/COM2 UARTs for error reporting and interactive commands.

2.1.4 Alpha SRM Console

The Alpha SRM Console firmware provides service functions commonly provided in most computer systems, including the following:

- I/O subsystem initialization
- Operator interface
- OS bootstrap and restart

API NetWorks, Inc.'s SRM Console firmware provides UNIX palcode for Linux and other suggested operating systems.

Note: *See the CS20 Technical Reference Manual, 51-0063-1A, or the API NetWorks Firmware Reference Guide, 51-0058-1A, for further details.*

Users communicate with the SRM Console with the COM1/COM2 serial ports. SRM Console firmware supports the use of the VT-style terminal attached to the standard serial ports.

SRM Console firmware provides a command line interface with a single UNIX-like shell that has a simple scripting facility.

Chapter 3 System Memory

This chapter gives an overview of the CS20 system memory. Valid memory configurations are included.

Note: *For details on system address mapping, memory DQM configuration, jumper settings, operating system loading information, and LEDs, see the CS20 Technical Reference Manual, 51-0063-1A.*

CAUTION: Always take appropriate electrostatic discharge safety measures when handling boards or modules.

3.1 Memory Subsystem

The CS20 system has eight DIMM sockets arranged in two banks: Bank 0 and Bank 1. Each bank has four sockets and provides a 256-bit wide data path.

The minimum memory size is 256 MB (four 64 MB DIMMs), and the maximum size is 2 GB (eight 256 MB DIMMs). The system clock is 83.3 MHz, yielding a maximum bandwidth of 2.67 GB/sec. System firmware automatically detects memory type and size.

The CS20 system supports the following:

- 168-pin, 100 MHz registered SDRAM DIMMs with ECC and SPD
- LVTTL-compatible inputs and outputs
- 3.3V +- 0.3V power supply

Note: *DIMMs installed in the same memory bank must be of the same type, size, and speed. DIMMs installed in different memory banks may differ between banks.*

3.2 Configuring SDRAM Memory

The CS20 supports memory sizes from 256 MB to 2 GB. Table 3-1 lists some of the SDRAM memory configurations available.

Note: *For a list of tested DIMMs, see the Hardware Compatibility List on API's web site at www.api-networks.com.*

.

Table 3-1 CS20 SDRAM Memory Configurations

Total Memory	Bank 0	Bank 1
256 MB	64 MB x 4	
512 MB	128 MB x 4	
	64 MB x 4	64 MB x 4
768 MB	128 MB x 4	64 MB x 4
1 GB	256 MB x 4	
	128 MB x 4	128 MB x 4
1.5 GB	256 MB x 4	128 MB x 4
2 GB	256 MB x 4	256 MB x 4

Note: *See the CS20 Quick Start Installation Guide, 51-0062-0B, for an illustration of memory installation for the CS20 system.*

Chapter 4 System Troubleshooting

This chapter discusses hardware and software troubleshooting for the CS20 system.

Note: *For details on system address mapping, memory DQM configuration, jumper settings, operating system loading information, and LEDs, see the CS20 Technical Reference Manual, 51-0063-1A.*

CAUTION: Always take appropriate electrostatic discharge safety measures when handling boards or modules.

4.1 Error Recovery

The CS20 system motherboard has a firmware configuration jumper block (J2) located on its left side just above J30, the IDE device port. It is an eight-position, 2-pin jumper block, as shown in Figure 4-1. This jumper block is used for troubleshooting and error recovery.

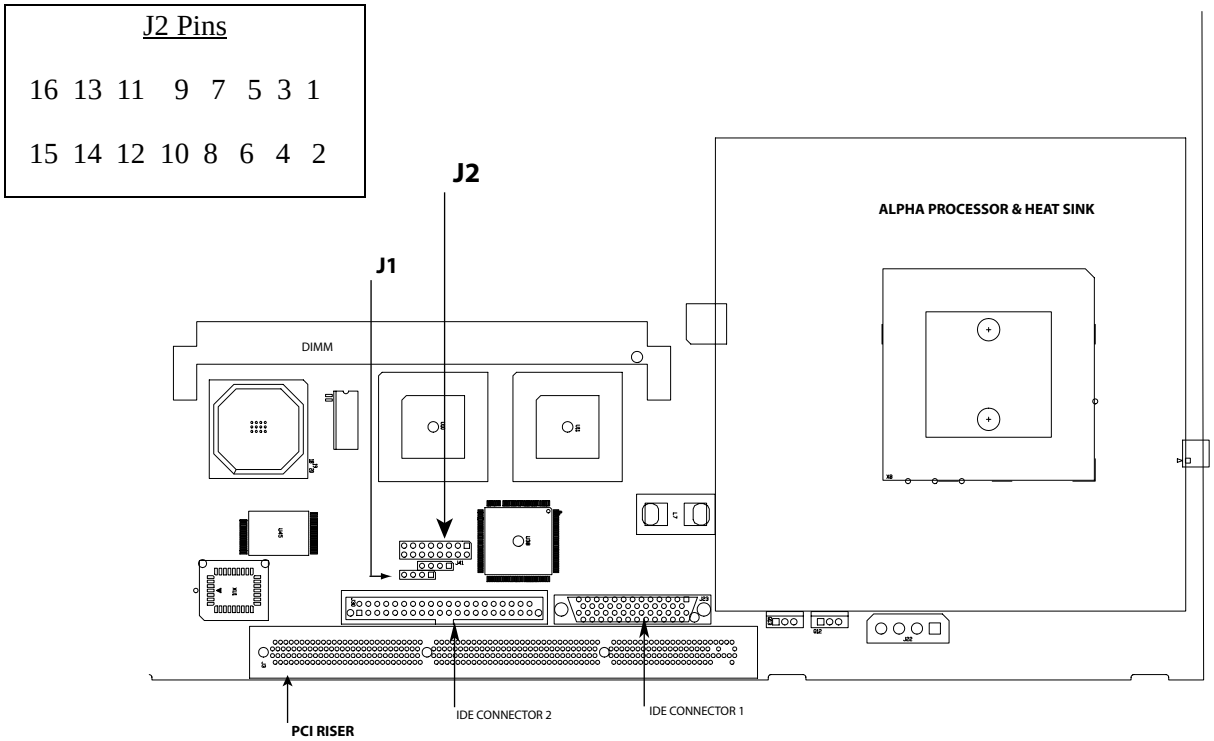

Figure 4-1 J2 Firmware Configuration Jumper Block

- J1 allows manual disabling of either or both processors on the CS20 system. J1 shunts are factory installed and are not user configurable. Both sets of pins shunted.

- J41 is the usual speaker connector, but it is not used on the CS20 and is reserved for factory testing.
- J2 pins 13-14 are the auxiliary I2C bus connector. The auxiliary I2C bus connector on the CS20 motherboard is not used in the CS20 system; it is reserved for factory or FRU testing.
- J2 pins 15-16 are factory set and are not user configurable.
- J2 pins 11-12, 9-10, and 7-8 are reserved.

For J2 pin configurations, see Figure 4-1.

For J2 pin functions, see Table 4-1.

For additional fail-safe mode information, see Table 4-2.

Table 4-1 J2 Pin Functions

Function	Install Jumper on Pins		
	5/6	**3/4**	**1/2**
Normal operations; execute firmware and boot to operating system using current or default environment settings.	0	0	0
Restore factory default environment settings.	0	0	1
Upgrade or recover firmware (COM1).	0	1	0
Failsafe reflash from CDROM (COM1).	0	1	1
Field installation and test mode.	1	*	*

Note: 0 = No jumper installed; 1= Jumper installed
***** *indicates reserved pins*

There are two push-button switches on the motherboard. SW1 is HALT and is accessible through an opening on the front panel of the system. SW2 (at J32) is RESET and is accessible when the system cover is removed.

4.1.1 Error Conditions

In addition to the factory default configuration setting, there are two other configuration settings that can be used for recovery from firmware errors. For more information, see the FAQs on the API NetWorks, Inc. website:

`www.api-networks.com`

4.1.2 Restore Factory Defaults

Some error conditions of this type include:

- Choosing incorrect selections when configuring the SRM console. These selections may prevent the system from booting.
- *Forgetting your system password.*

For recovery from these types of errors, install a jumper on pins 15 and 16 of J2 to invoke the fail-safe boot-recover procedure.

4.1.3 Reload Firmware

An error condition of this type may occur during the upgrading of the SRM console by an improper system action. An example may consist of accidentally powering off the system during this procedure.

For this type of recovery, install a jumper on pins 1 and 2 of J2 to override these errors.

4.1.4 Error Recovery Procedure

To clear the errors noted in Section 4.1.1, follow these steps:

1. Power off the system.
2. Change the jumper shunt according to the area to be cleared. See Table 4-2.
3. Start the system.
4. Enter the proper parameters in the SRM console, and then load the operating system.
5. Power off the system.
6. Restore the jumper shunts to their default positions.
7. Start the system.

Table 4-2 Jumper Settings for Error-Recovery Procedures

Function	Install Jumper on Pins		
	5/6	**3/4**	**1/2**
Restore factory defaults	0	0	1
Recover firmware	0	1	0
Failsafe reflash from CDROM (COM1).	0	1	1

Note: 0 = No jumper installed; 1= Jumper installed

Appendix A

Resources

A.1 Customer Support

API NetWorks, Inc. provides product assistance on our web page at:

`www.api-networks.com`.

Alpha Original Equipment Manufacturers (OEMs) provide the following web-page resources for customer support:

URL	Description
`www.compaq.com`	Contains links for the 21272 chipset.

A.2 Supporting Products

API NetWorks, Inc. maintains a Hardware Compatibility List on the `http://hcl.api-networks.com` website for components and accessories that are not included with the CS20. Compatibility for items such as memory, power supplies, and enclosure are listed.

Point your browser to `www.api-networks.com`, and check the Product Information list for peripherals.

A.3 Alpha Products

API NetWorks, Inc. maintains information about other Alpha products on `www.api-networks.com`, and check the Product Information list for Alpha products.

A.4 Documentation

A.4.1 Alpha Documentation

Title	Vendor
Alpha Architecture Reference Manual, Third Edition	Compaq Computer Corporation, Digital Press order# EQ-W938E-DP
Alpha Architecture Handbook, Version 4	Compaq Computer Corporation Digital Press order# EC-QD2KC-TE
AlphaPC 264DP Technical Reference Manual	Compaq Computer Corporation, Digital Press order# EC-RBODA-TE

A.4.2 Third-Party Documentation

You can order the following associated documentation directly from the vendor:

Title	Vendor
• *PCI Local Bus Specification, Revision 2.1* • *PCI Multimedia Design Guide, Revision 1.0* • *PCI System Design Guide* • *PCI-to-PCI Bridge Architecture Specification* • *PCI BIOS Specification, Revision 2.1*	PCI Special Interest Group U.S. 1-800-433-5177 International1-503-797-4207 FAX 1-503-234-6762
Computer Architecture	John L. Hennessy and David A. Patterson, Morgan Kaufman Publishers, San Mateo, CA, 1990

Index

A

Adaptec AIC-7892, 1-2
Alpha 21264 processors, 1-6
Alpha Architecture Handbook, A-2
Alpha Architecture Reference Manual, A-2
Alpha Diagnostics, 1-2, 2-1
  supported versions, 2-1
Alpha publications, A-2
Alpha SRM Console, 2-1
  command line interface, 2-2
  communication access, 2-2
  firmware design, 2-2
  supported versions, 2-1
Alpha SRM Console firmware, 2-1
AlphaPC 264DP Technical Reference Manual, A-2

B

banks
  memory, 3-1
bezel, 1-3

C

cache, 1-2
  Icache
    SROM code firmware design, 2-1
    SROM code images, 2-1
central processing units (CPUs), 1-3
chipset, 1-2
CLI
  Alpha SRM Console, 2-2
components
  system, 1-3
Computer Architecture, A-2
configuration
  memory, 3-1
configuration jumpers, 2-1
conventions, x
  abbreviations, xi
  acronyms, xi
  addressing, xi
  data, x
  reserved bits and signals, x
  signal ranges, x

units, x
CPU (central processing unit), 2-1
CS20
Alpha SRM Console, 2-2
memory
configurations supported, 3-2
specification, 3-1
SROM code firmware, 2-1
supported firmware versions, 2-1
supported OS, 2-1
customer support, A-1

D

data path
memory subsystem capacity, 1-5
debug
ports, 2-1
default
restore environment settings, 4-2
definitions, conventions, and references, x
DIMM
configuration rules, 1-5
memory subsystem, 1-5
disabling
manual, 4-1
disk carrier, 1-3
Double Data Rate (DDR) transfers, 1-2

E

electrostatic precautions, 4-1
enclosure
system, 1-3
environment settings, 4-2
error conditions, 4-2
error recovery, 4-1
error recovery procedure, 4-3
external L2 cache, 1-2

F

failsafe reflash from CDROM, 4-2
fans
system, 1-3
features
product, 1-1
system, 1-1
firmware, 1-2
memory auto detection, 3-1
supported, 2-1
supported versions, 2-1
firmware configuration jumper block, 4-1
form factor, 1-2

H

hardware
troubleshooting, 4-1
Hardware Compatibility List (HCL), A-1

I

I/O board, 1-6
I/O slots, 1-2

J

J1, 4-1
J2, 4-2
jumper block
firmware, 4-1
jumper pins
factory set, 4-2
factory testing, 4-2
reserved, 4-2

L

LED
internal power failure, 1-5
Red, 1-5
Linux, 2-1

M

main memory, 1-2
memory
bandwidth, 3-1
bank arrangement, 3-1
configuration, 3-1, 3-2
rules, 1-5
DIMM, 3-1
size, 3-1

subsystem description, 1-5
memory subsystem, 3-1
motherboard
memory
configuration, 1-6
subsystem description, 1-5

O

on-board I/O, 1-2
operating system, 2-1
supported OS, 2-1
OS support, 2-2

P

PCI BIOS Specification, Revision 2.1, A-2
PCI Local Bus Specification, Revision 2.1, A-2
PCI Multimedia Design Guide, Revision 1.0, A-2
PCI riser, 1-6
PCI System Design Guide, A-2
PCI-ISA Bridge I2C controller, 1-3
PCI-to-PCI Bridge Architecture Specification, Revision 0, A-2
physical dimensions, 1-3
physical form factor, 1-2
pin functions
COM1, 4-2
field installation, 4-2
normal, 4-2
recover firmware, 4-2
restore factory default, 4-2
test mode, 4-2
upgrade firmware, 4-2
ports
debug, 2-1
power
system, 1-2
power failure
internal, 1-5
power supply, 1-3
precautions
electrostatic, 4-1
processors
Alpha 21264, 1-6
product features, 1-1
publications
related, A-2

R

related publications, A-2
reset
internal power failure, 1-5

S

sockets
DIMM, 3-1
software troubleshooting, 4-1
SROM, 1-2
SROM code, 2-1
firmware functional description, 2-1
supported versions, 2-1
subsystem
memory, 3-1
supported firmware, 2-1
supporting products, A-1
Symbios 53C1000, 1-2
system
clock
memory bandwidth, 3-1
components, 1-3
front view, 1-3
motherboard, 1-5
rear view, 1-4
system components, 1-3
system features, 1-1
system management, 1-3
system power, 1-2

T

target operating system (OS), 2-1
testing, 4-2
troubleshooting
hardware, 4-1
software, 4-1

U

Ultra160 SCSI Controller, 1-2